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VI Semester B.Voc.(IT) Degree Examination, September - 2021
COMPUTER ARCHITECTURE
(CBCS Scheme)
Paper : F022

Time : 3 Hours **Maximum Marks : 70**

Instructions to Candidates:

Answer **ALL** sections.

SECTION - A

I. Answer any **TEN** questions. **(10×2=20)**

1. State Demorgan theorem.
2. Write truth table for Full adder.
3. What is stable state?
4. Find 9's and 10's complement of 56483.
5. What do you mean by fixed point representation?
6. Define Register.
7. Define CIL instruction.
8. What is effective address?
9. Define Polling.
10. What are the various causes of internal interrupt?
11. Define Hit ratio.
12. What do you mean by polling?

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SECTION - B

II. Answer any **FIVE** questions. **(5×10=50)**

13. a. What is Half adder? Draw the logic diagram and truth table of Half adder. **(5)**
    b. What is decoder? Explain 3×8 decoder with a neat diagram. **(5)**

14. a. Discuss about SR flip flop. **(4)**
    b. Explain 4 bit parallel load register with a neat diagram. **(6)**

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15. a. Explain parity generator and parity checker with a diagram. (5)

b. Explain the different types of data transfer operations. (5)

16. a. Explain self complementing, weighted and excess 3 code with an example. (5)

b. Explain the basic computer's instruction code formats. (5)

17. a. Explain the operation of interrupt cycle with flowchart. (5)

b. Explain timing and control unit of basic computer. (5)

18. a. Compare RISC and CISC. (5)

b. Explain any five addressing modes with example. (5)

19. a. Explain the status bit register of CPU. (5)

b. Explain the working of DMA controller. (5)

20. a. Explain handshaking operations using source initiated. (5)

b. Briefly explain cache memory. (5)

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